

8

7

6

5

4

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2

1

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REVISIONS

REV

DESCRIPTION

DATE

APPROVED

SDP-K1 SCHEMATIC

PAGE 2 - USB

PAGE 3 - MCU

PAGE 4 - MCU MISCELLANEOUS SIGNALS

PAGE 5 - PROGRAMMING PROCESSOR

PAGE 6 - POWER ON RESET

PAGE 7 - POWER CIRCUITRY

PAGE 8 - ARDUINO UNO REV3 HEADER

PAGE 9 - SDP CONNECTOR

PAGE 10 - SDRAM LEVEL TRANSLATORS

PAGE 11 - SDRAM

P.O SPEC.

BK/BD SPEC.

SOCKET OEM

OEM PART#

HANDLER

TEMPLATE ENGINEER

-

HARDWARE SERVICES

-

HARDWARE SYSTEMS

-

TEST ENGINEER

-

COMPONENT ENGINEER

-

TEST PROCESS

-

HARDWARE RELEASE

-

DESIGNER

-

PTD ENGINEER

Sean Doyle

CHECKER

-

DATE

SCHEMATIC

HW TYPE : Customer Evaluation

Product(s): N/A

: N/A

PACKAGE : N/A-lead N/A N/A-family

: Pitch-pitch StyleVendor Style

<User Define>

<User Define>

<User Define>

MASTER PROJECT TEMPLATE

TBD

TESTER TEMPLATE

no\_template

DRAWING NO.

02\_049259

REV.

F

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES

DECIMALS

X.XX +0.010

X.XXX +0.005

FRACTIONS

+1/32

ANGLES

+2

SIZE

D

SCALE

1:1

CODE ID NO.

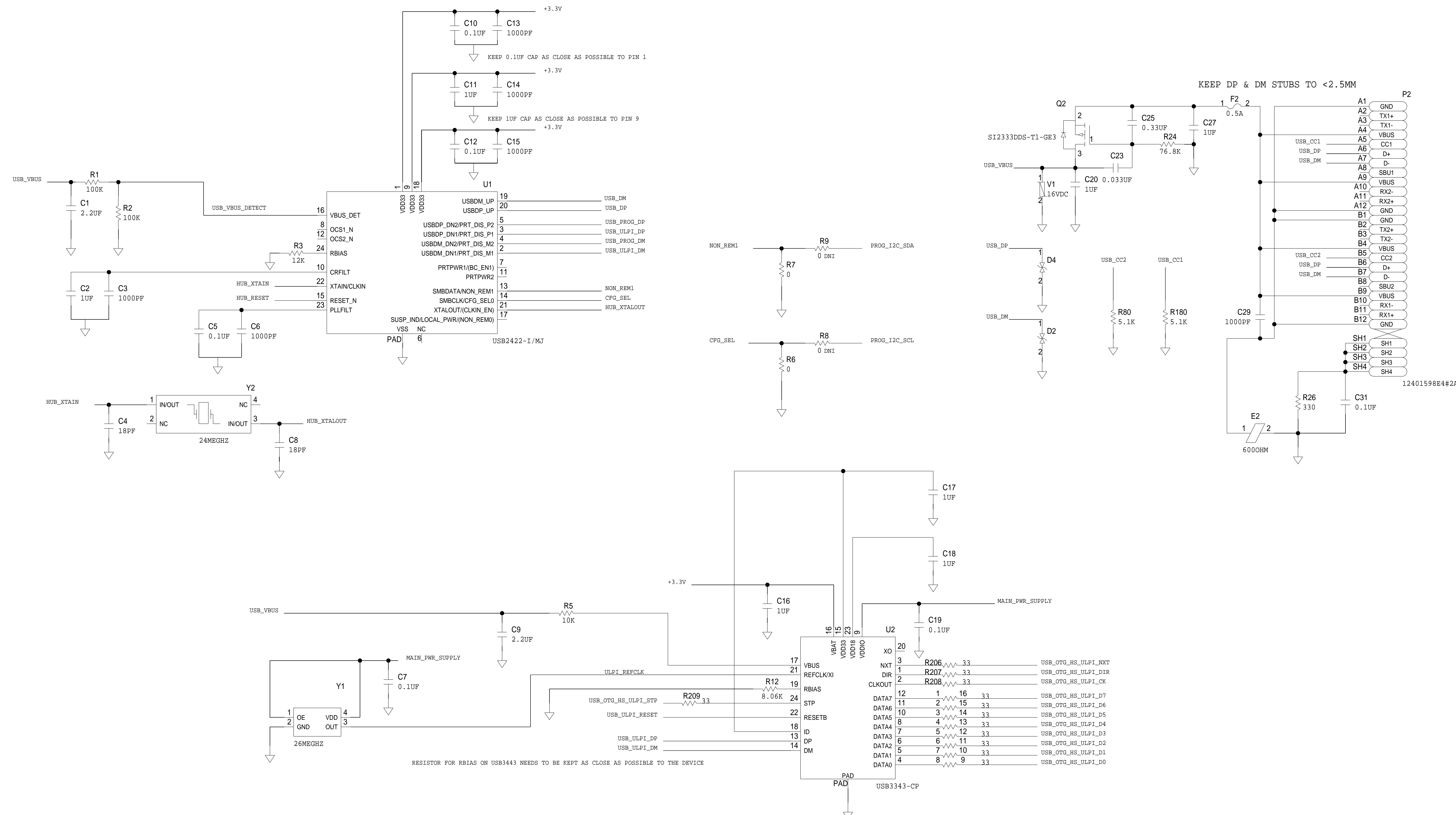
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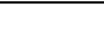
SHEET 1

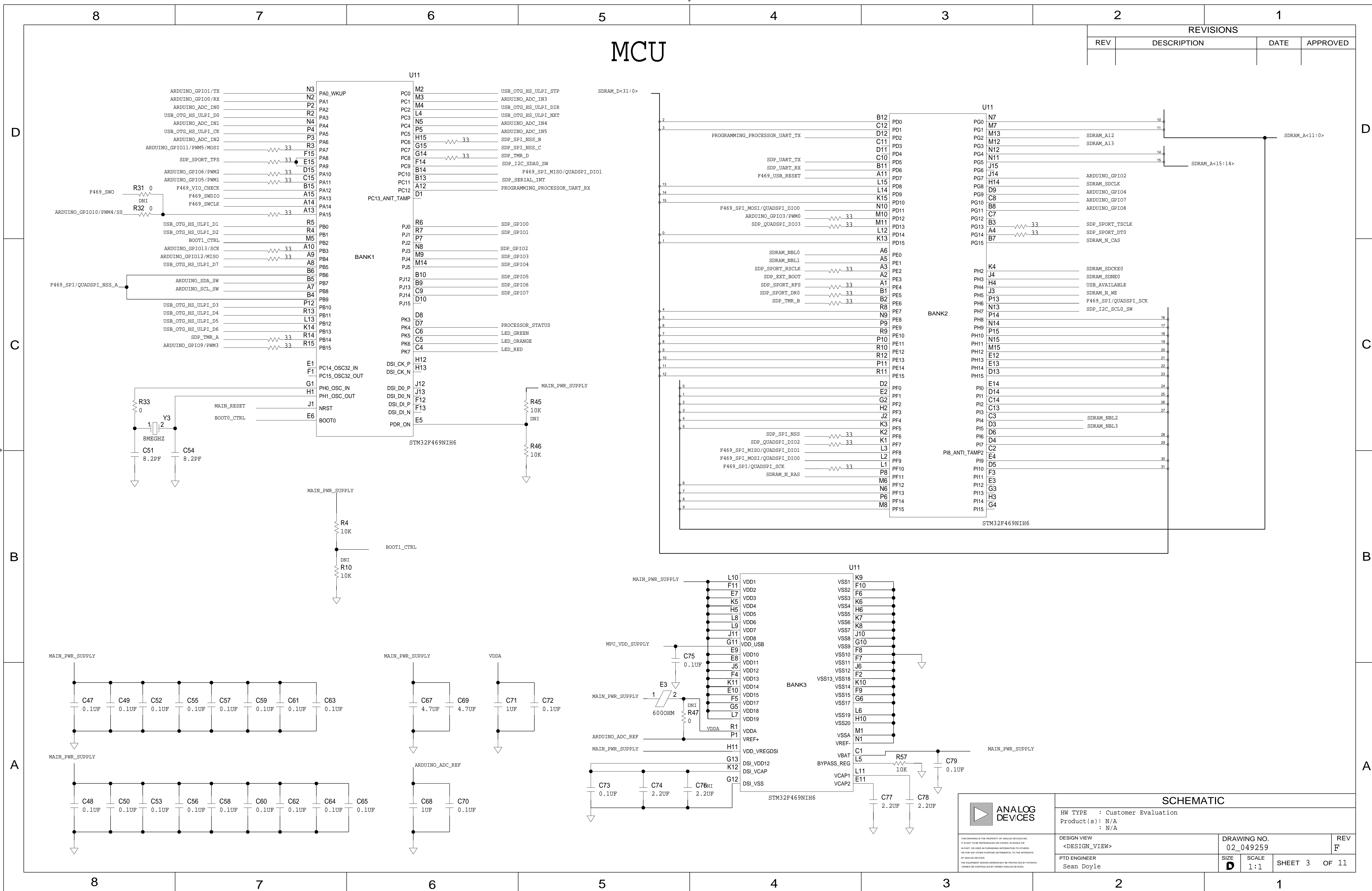
OF 11

# USB

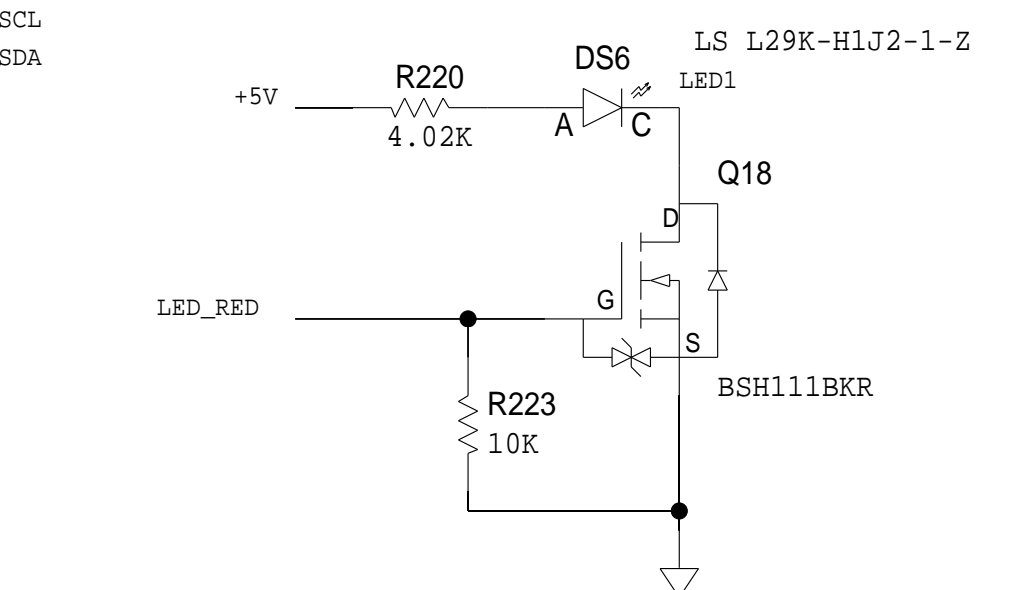
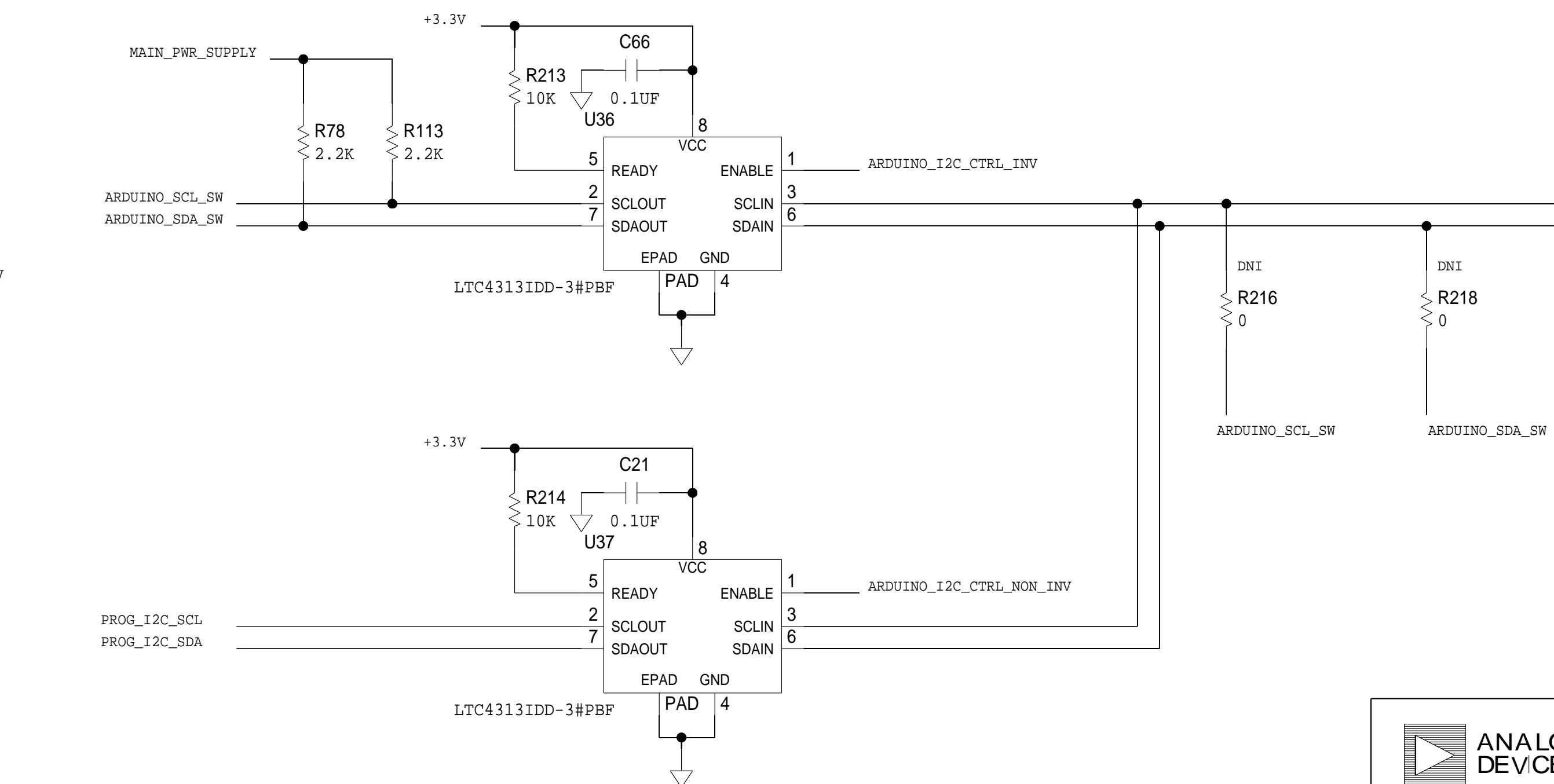
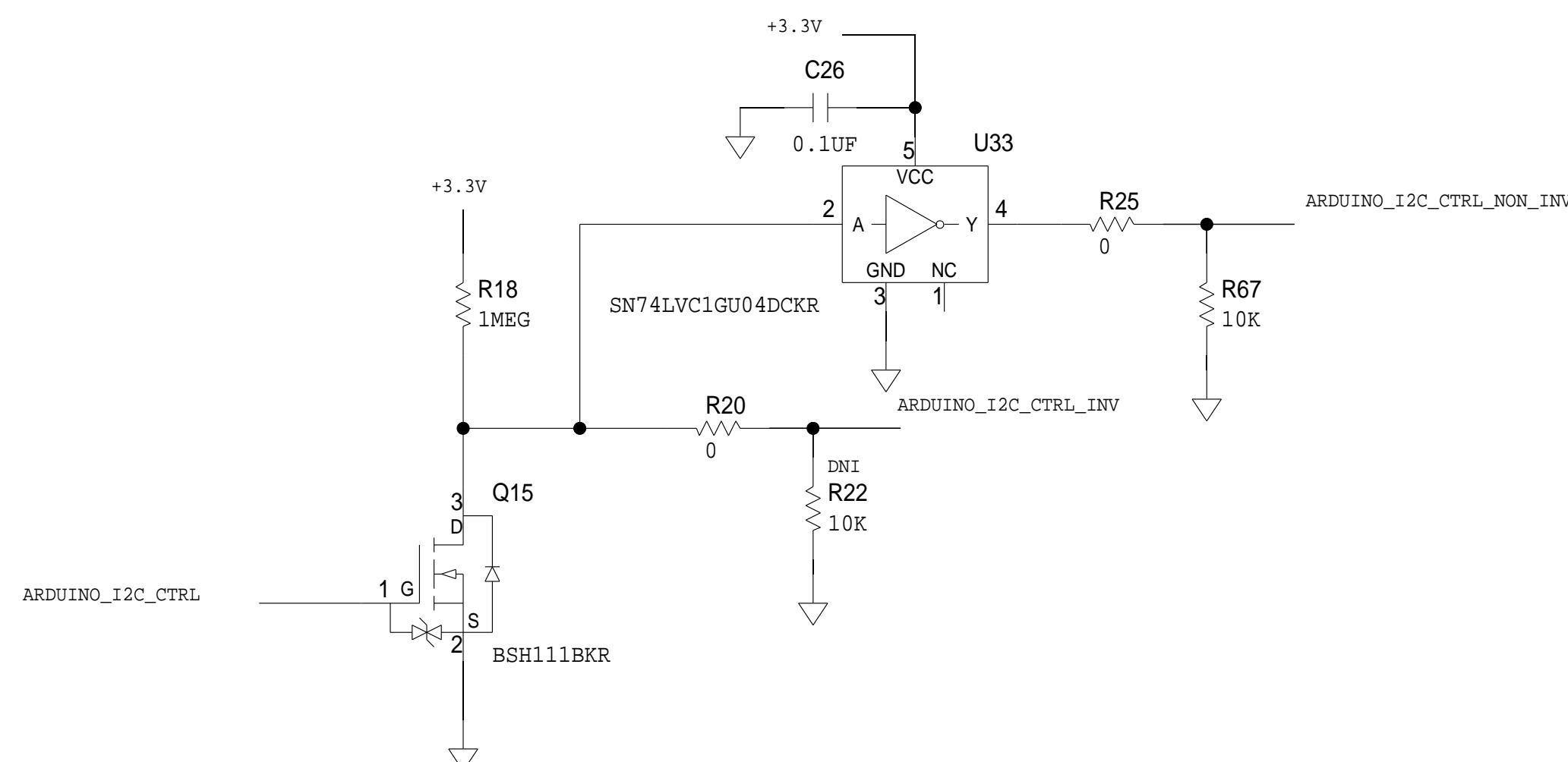
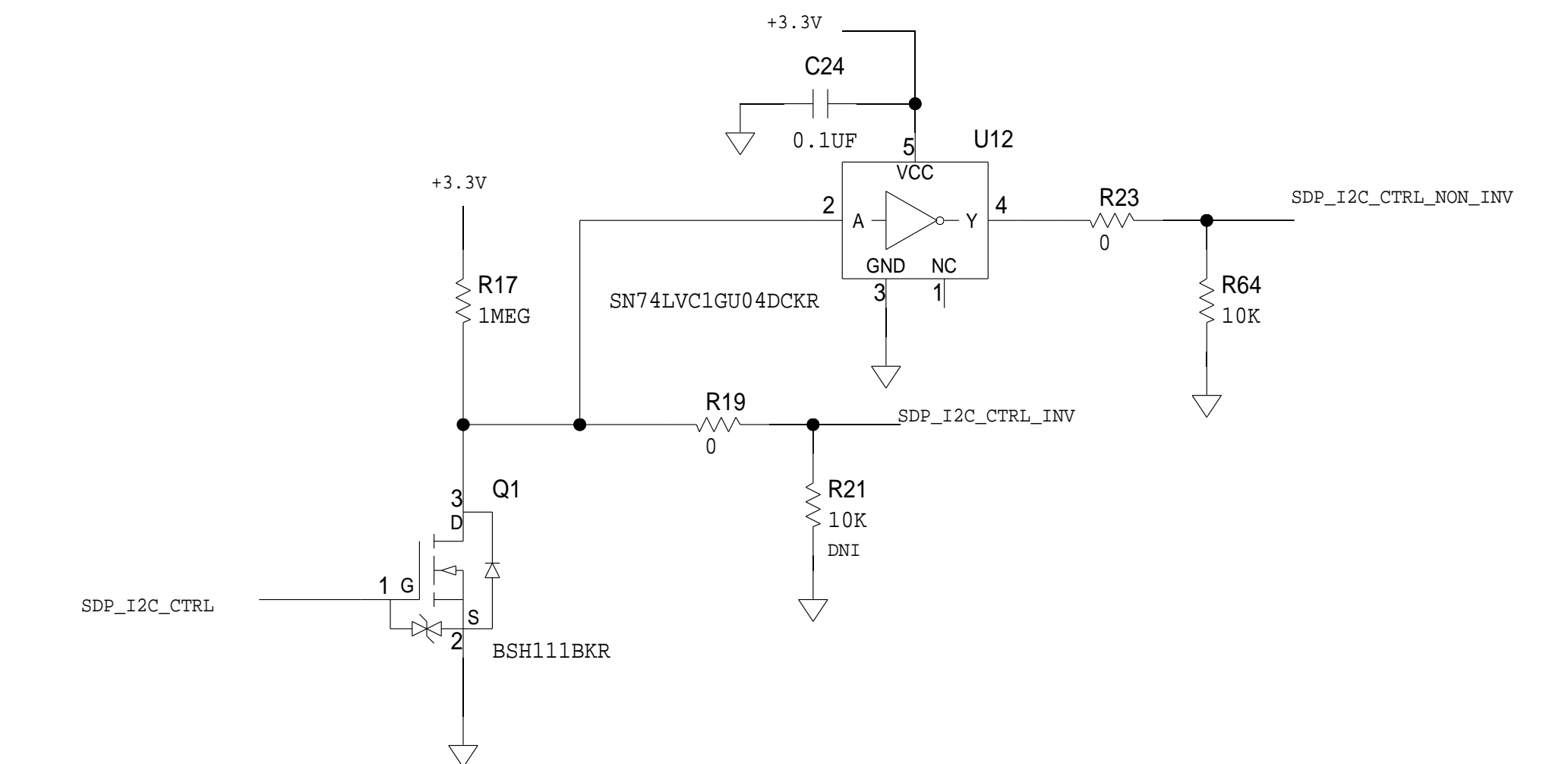
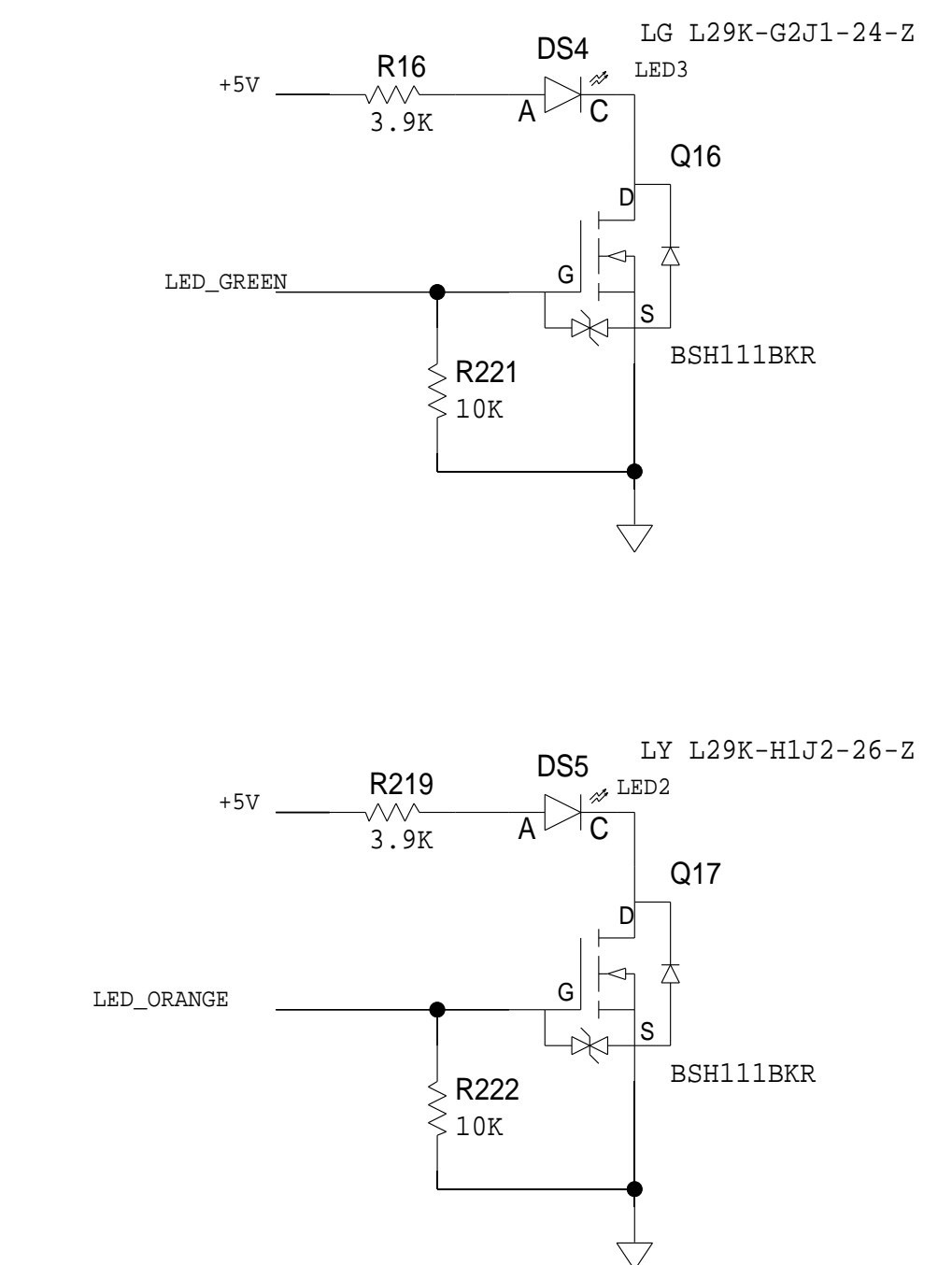
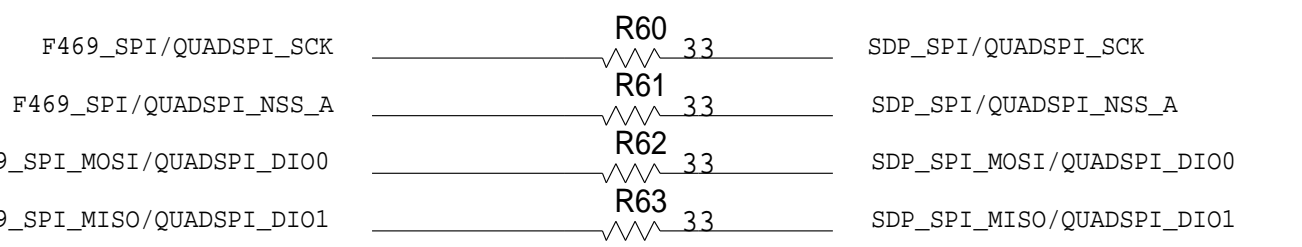
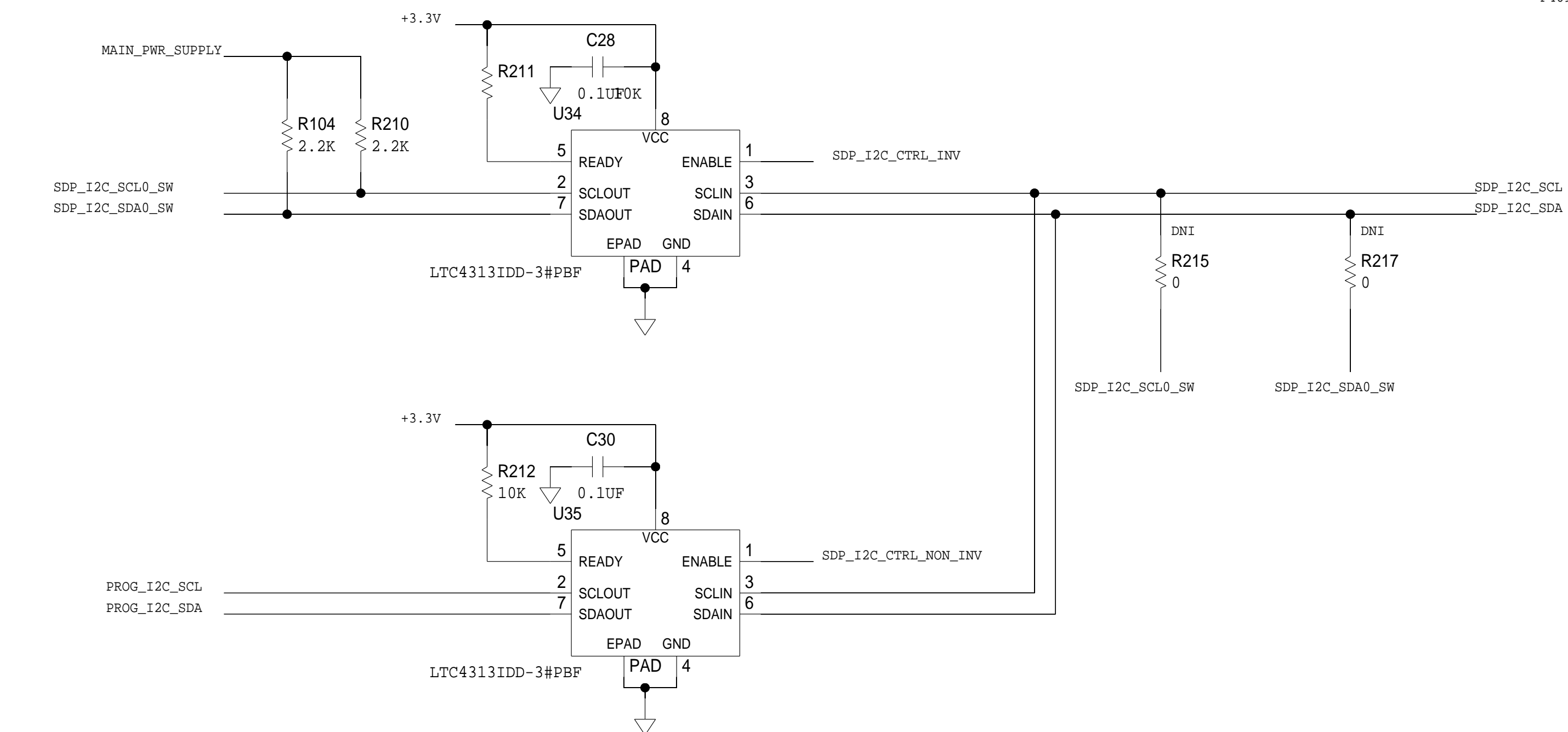
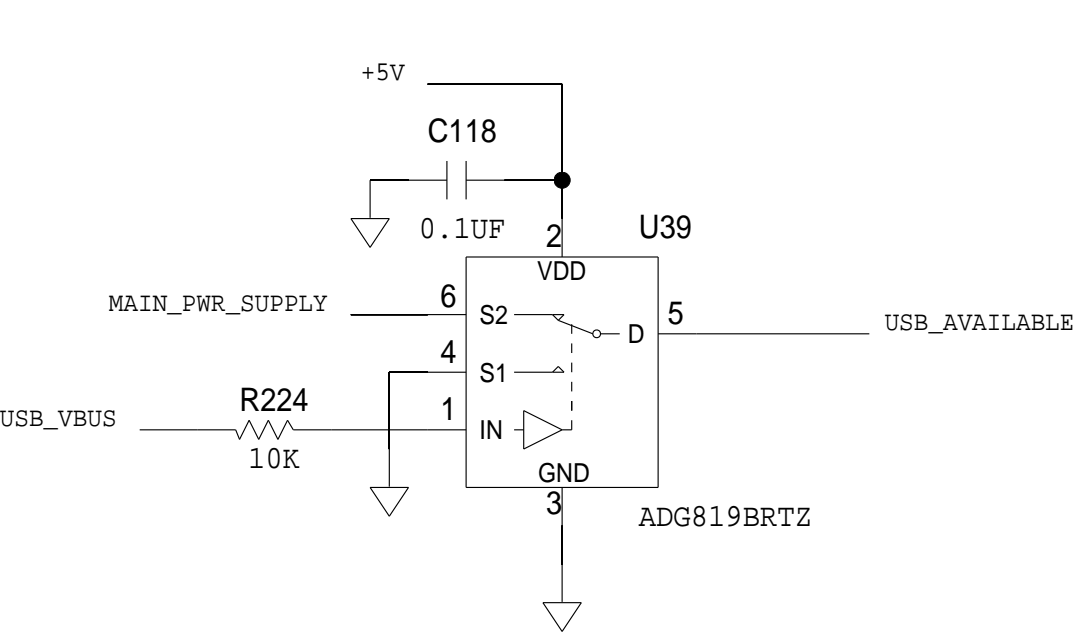
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED




 <b>ANA LOG DEVICES</b>	<h1 style="text-align: center;">SCHEMATIC</h1>			
	HW TYPE : Customer Evaluation Product(s) : N/A : N/A			
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<b>PTD Engineer</b> <b>Sean Doyle</b>	<b>SIZE</b> <b>D</b>	<b>SCALE</b> <b>1:1</b>	<b>SHEET</b> <b>2</b>	<b>OF</b> <b>11</b>



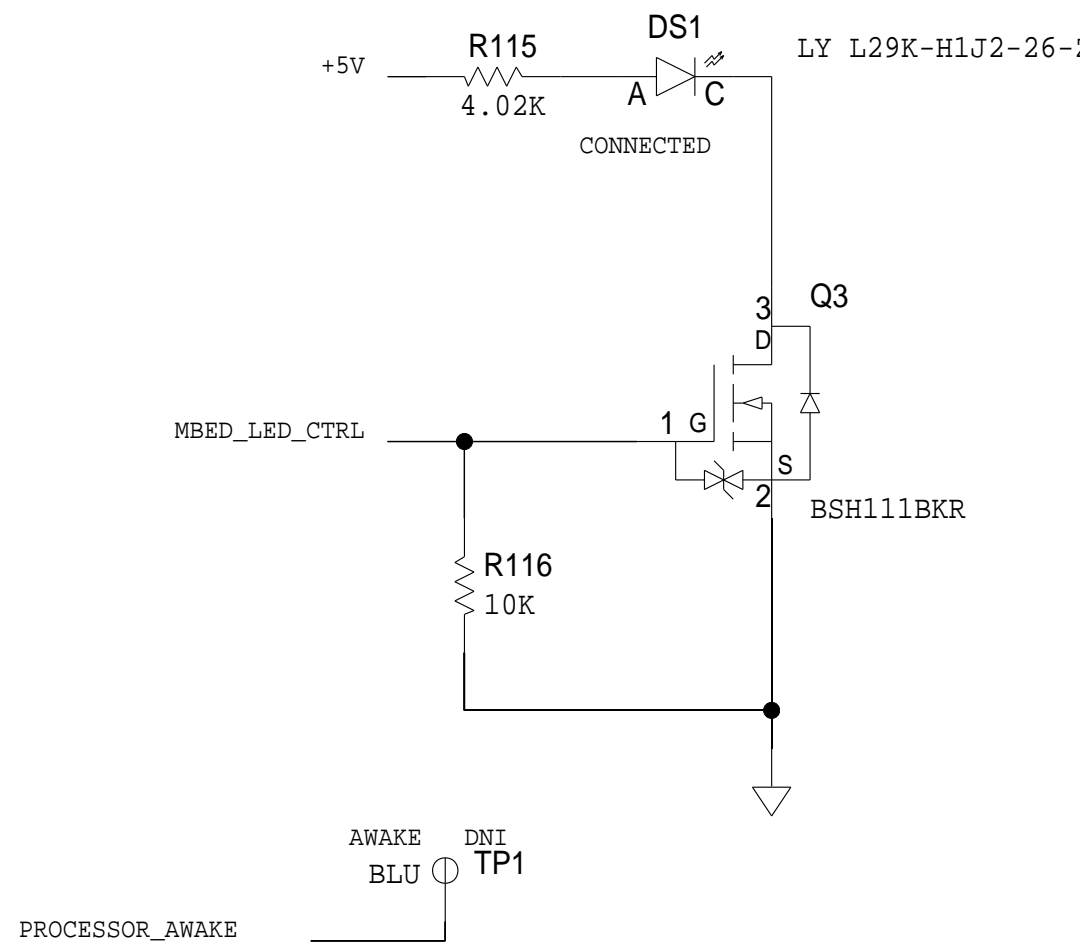
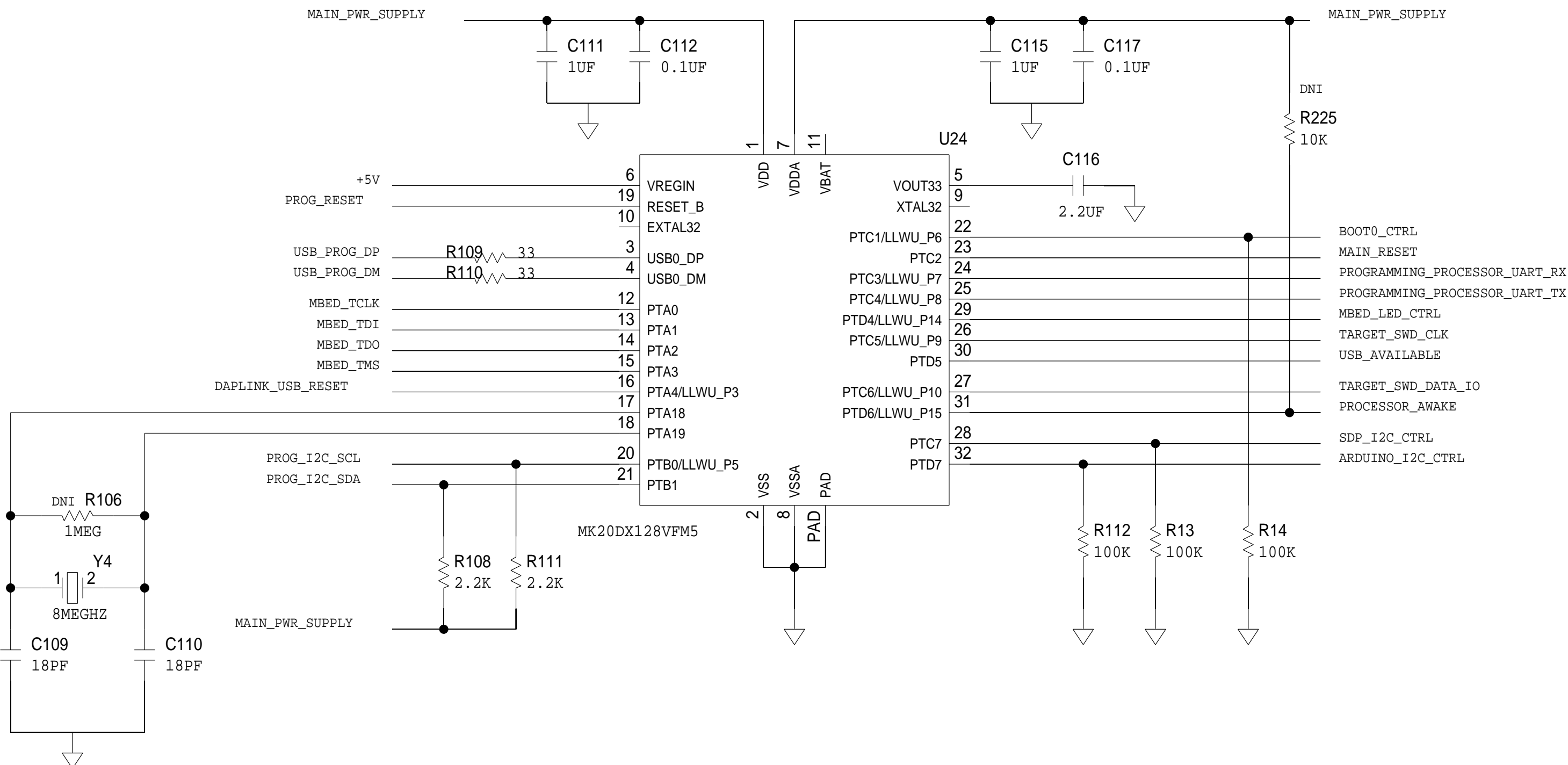
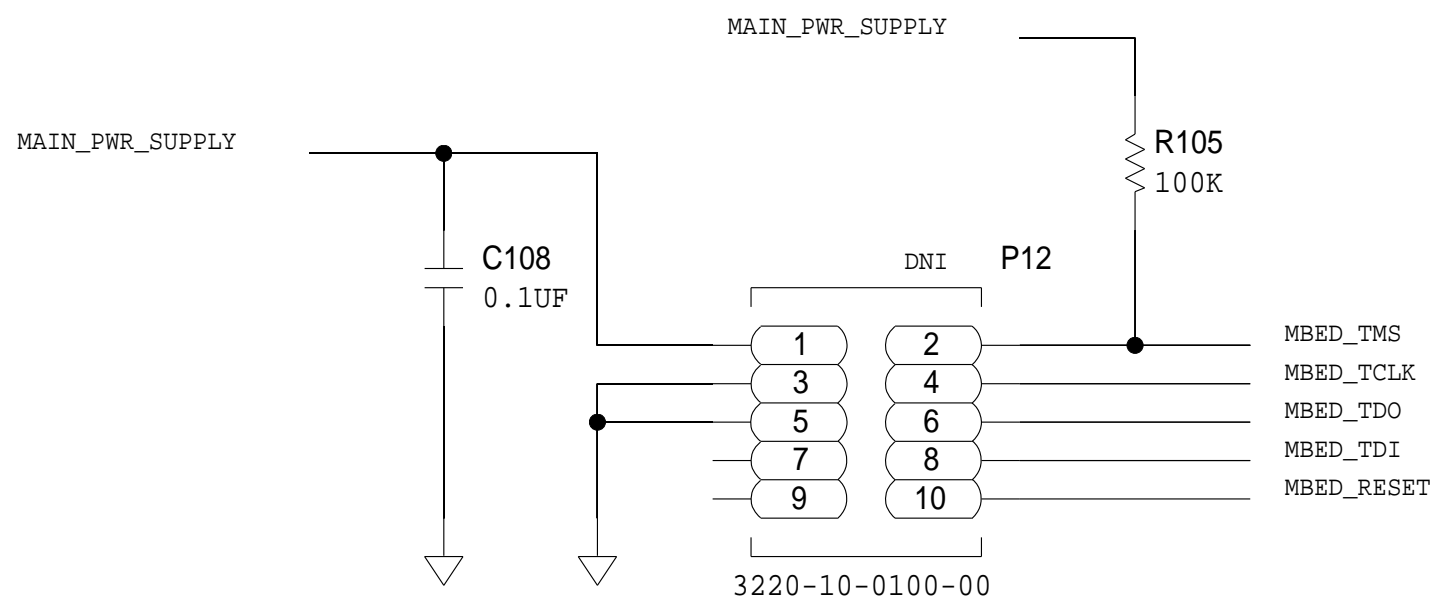
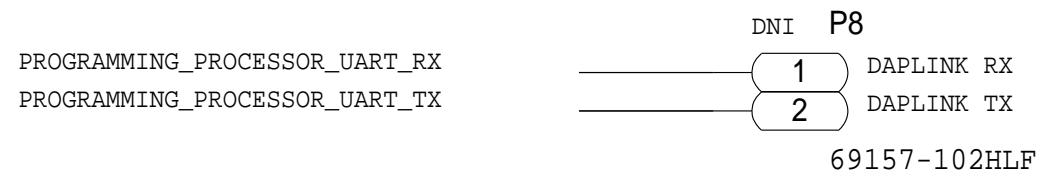
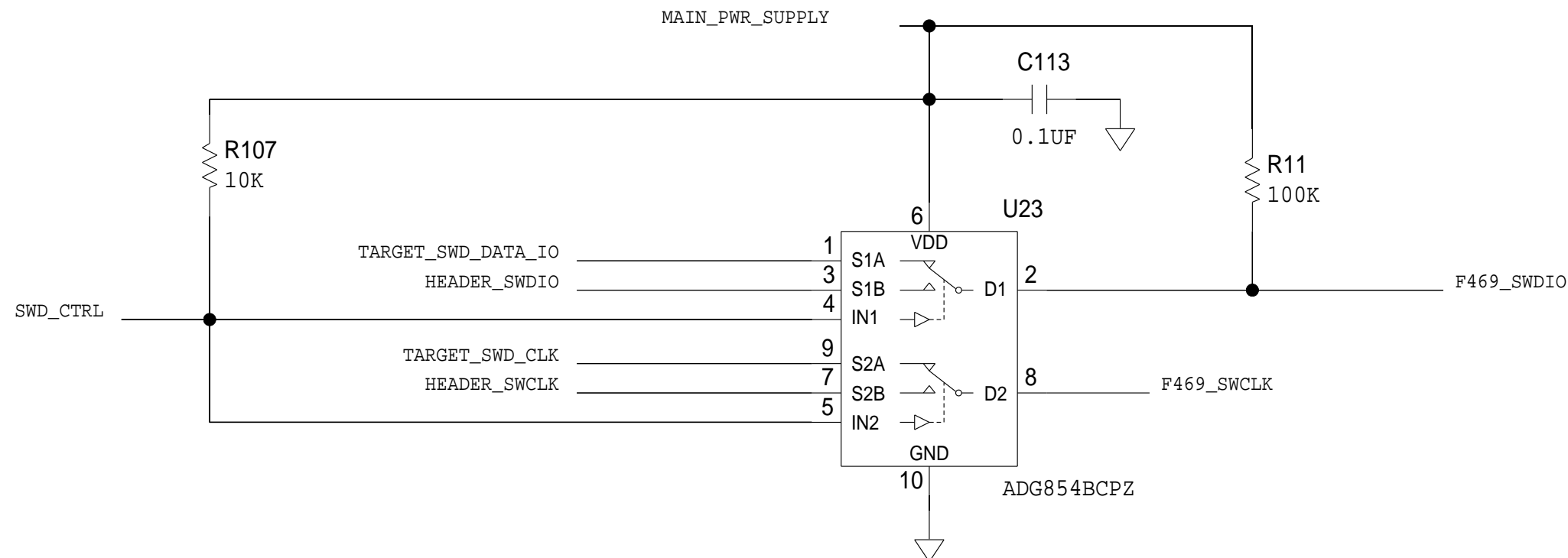
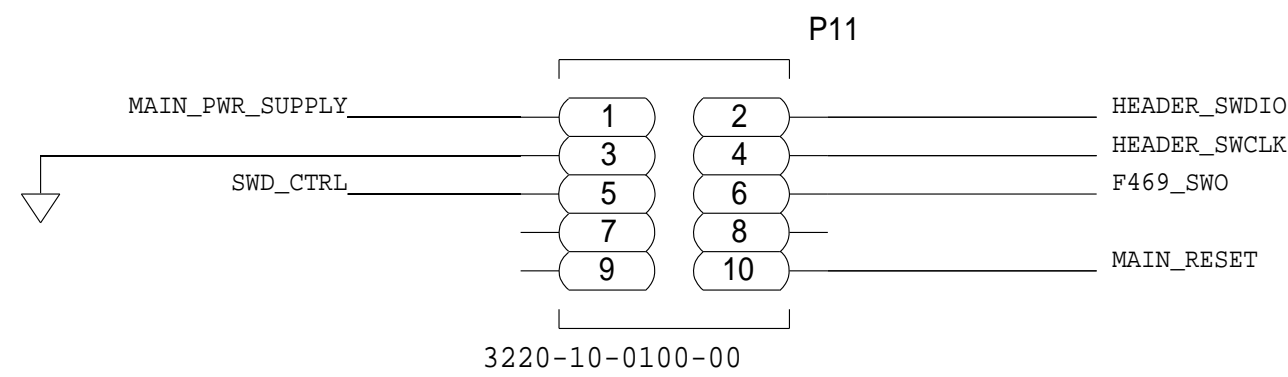
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

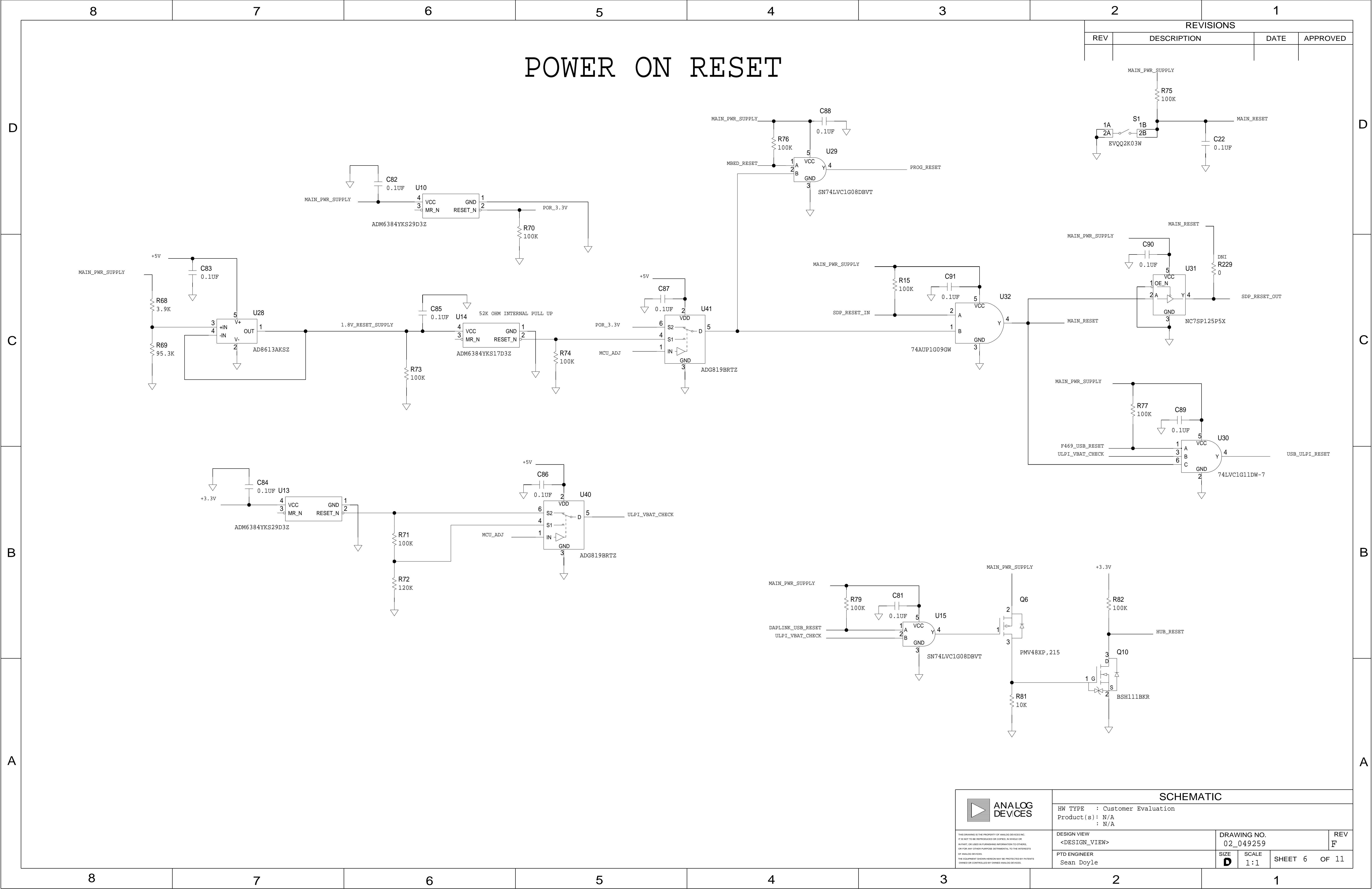


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	PTD ENGINEER <b>Sean Doyle</b>		SIZE <b>D</b>	SCALE <b>1:1</b>	SHEET <b>4</b> OF <b>11</b>

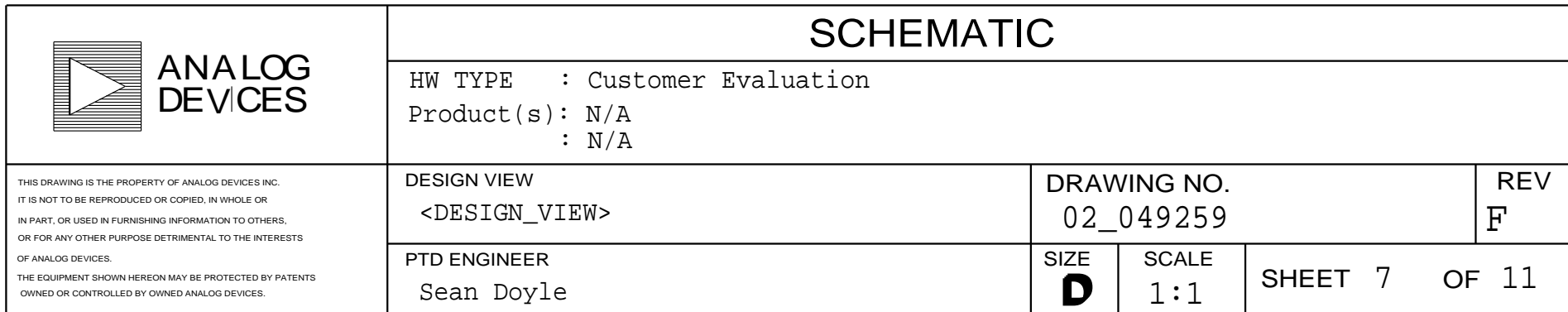
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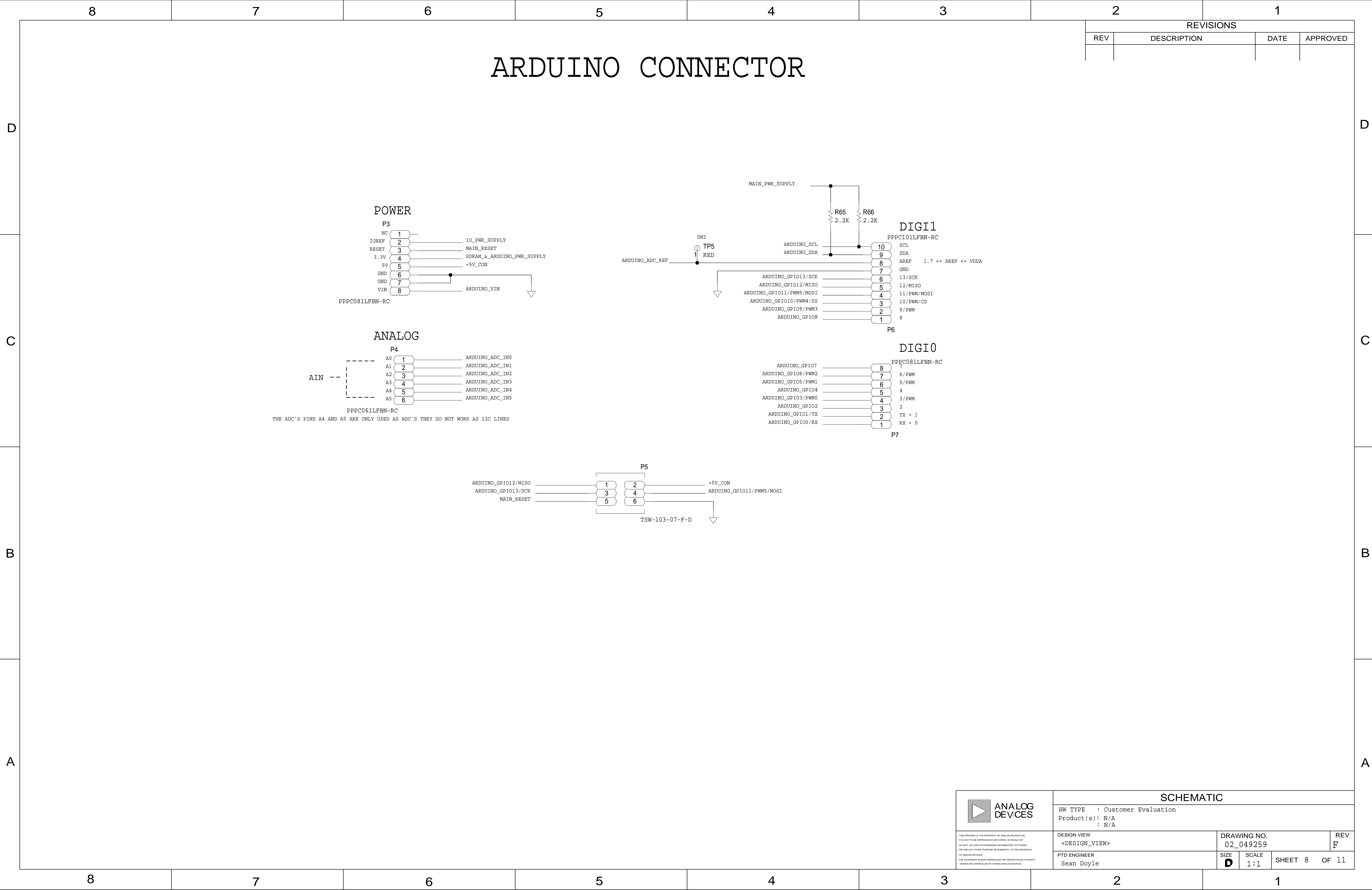
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED





REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

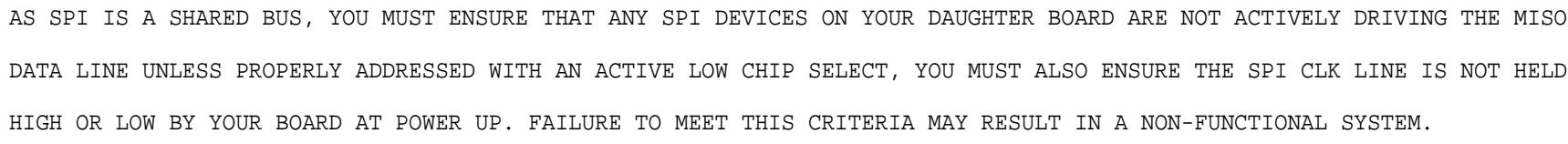




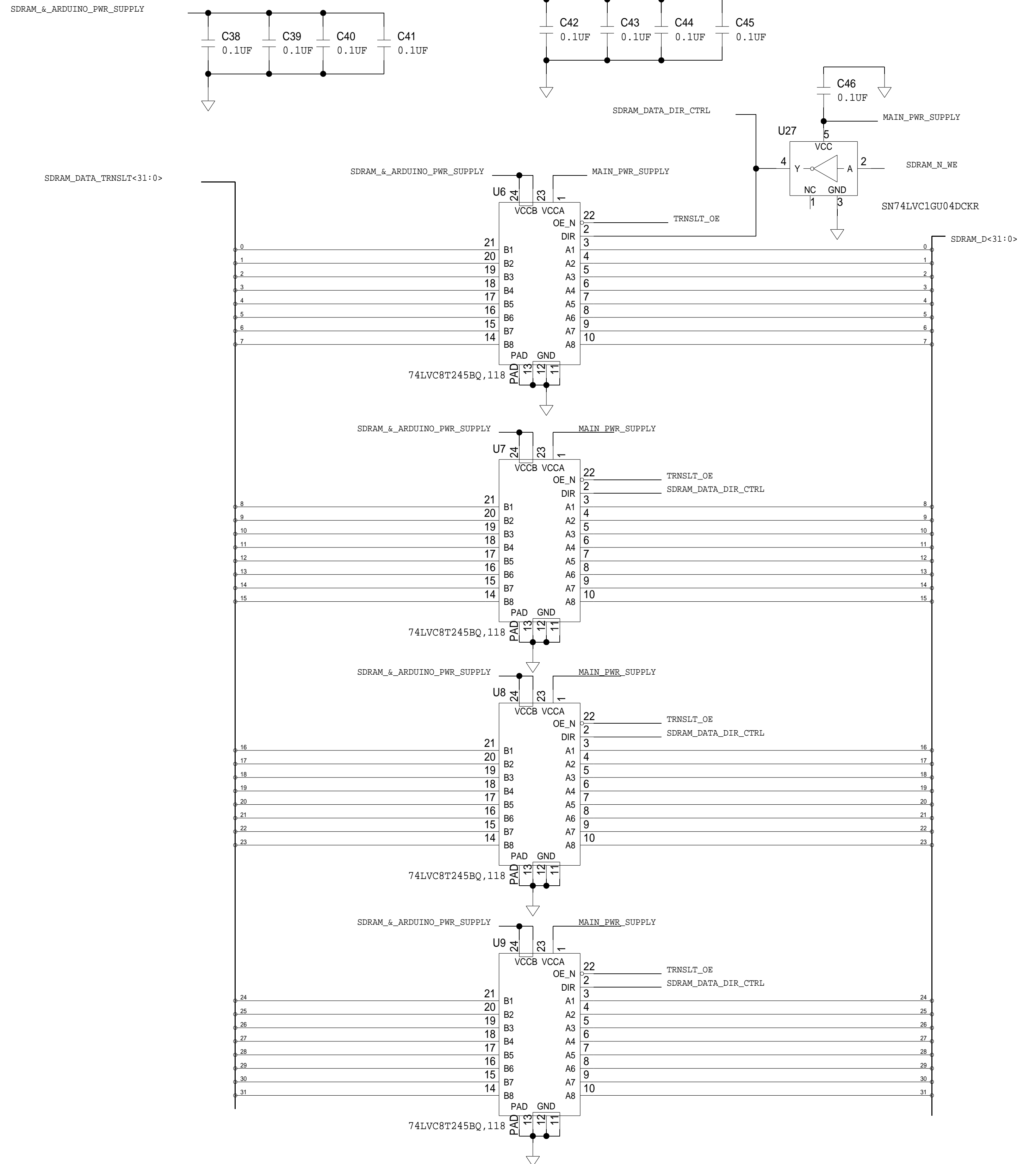



REVISIONS			
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WHEN DESIGNING A DAUGHTER BOARD THE ID EPROM (24LC32) MUST BE ON I2C BUS 0.  
CARE MUST BE TAKEN TO ENSURE DAUGHTER BOARD I2C EPROM ADDRESS  
IS NOT 0X50 OR 0X51. THIS IS TO ENSURE THE I2C ADDRESS RANGE DOES  
NOT OVERLAP THAT OF THE E13 BREAK-OUT BOARD.



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



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<b>PTD Engineer</b> <b>Sean Doyle</b>	<b>SIZE</b> <b>D</b>	<b>SCALE</b> <b>1:1</b>	<b>SHEET 10 OF 11</b>	

